Tutorial exercises No 2

Exercise 01:

1. What type of architecture does the 8086 have? (CISC or RISC).
2. In which year was the 8086 manufactured?
3. How many pins does the 8086 have?
4. What is the total number of registers in the 8086?
5. Name the segment registers, and where are they located in the microprocessor?
6. Name the index registers, and where are they located in the microprocessor?
7. What is the size of the microprocessor 8086's queue, and where is it located within the microprocessor?
8. What is the size in bytes of the memory addressable by the 8086?
9. An instruction consists of two fields, name them.
10. Which unit of the microprocessor is responsible for loading the physical address (20 bits) onto the address bus?

Exercise 02:

Answer the following statements with (true) or (false):

1. A segment is a memory area of 64 KB.
2. The flags that make up the status register are independent of each other.
3. The segment registers CS, DS, ES, and SS are responsible for selecting different memory segments by pointing to the beginning of each one.
4. The EU (Execution Unit) has no connection to the buses (address, data, and control).
5. The BIU (Bus Interface Unit) is responsible for filling the queue with fetched instructions.
6. The IP register contains the address of the memory location where the next instruction to be executed is located.
7. The parity flag PF is set to 1 if the result of an operation is even.
8. The BIU fetches instructions to be executed from memory and stores them in the 8086's queue.
9. The BIU calculates physical addresses in 16 bits.
10. Machine language is the only language that the processor can process.
11. The stack segment is organized in bytes (8 bits).
12. The PUSH instruction increments the address contained in the SP register by 2.
13. The Instruction Register (IR) can be manipulated by the programmer.

Exercise 03:

1. If the code segment register CS contains the value 2300H, determine the physical address of the start and end of the code segment.
2. If the data segment register DS contains the value 0100H, determine the physical address of the start and end of the data segment.
3. After the execution of the instructions below, provide the state of the flags (CF, ZF, SF, and PF) in the status register (flag register).

c)
```
mov  AX, 70D
mov  BX, 200D
add  AX, BX
```

b)
```
mov  AX, 22H
mov  BX, 52H
sub  AX, BX
```

d)
```
mov  AX, 22H
mov  BX, AX
sub  AX, BX
```

4. Consider the following assembly program segment

```
Mov    cx, 55h        ; The SP register contains the value 2244H.
Push   ax
Push   bx
Push   cx
```

Pop ax

Determine the contents of the SP and AX registers after the program execution.

Exercise 04 :

Choose the correct answer

1. The primary role of 'cache memory' is
   - **a)** to increase the storage capacity of main memory.
   - **b)** to compensate for slow speed and speed up access to main memory.
   - **c)** to improve the microprocessor's clock.
2. The execution time of an instruction depends on:
   - **a)** the complexity of the instruction and addressing mode.
   - **b)** the microprocessor's architecture.
   - **c)** the size of main memory.
3. The opcode of an instruction allows to:
   - **a)** determine its nature
   - **b)** locate the operand in memory.
   - **c)** indicate the type of operands.
4. In the stack segment:
   - **a)** the first element introduced is always the first one to be removed.
   - **b)** the first element introduced is always the last one to be removed.

Exercise 05 :

After executing the program below, determine the contents of registers AX, BX, and CX.
Determine the contents of register SP at the specified positions. Knowing that initially, SP contains FFFEH.

```
MOV  AX, 1122H
MOV  BX, 3344H
MOV  CX, 5566H
PUSH AX
PUSH BX ;Determine the content of the SP register after the execution of the current instruction SP = … ?
PUSH CX
POP  BX
POP  AX ;Determine the content of the SP register after the execution of the current instruction SP = … ?
POP  CX
```