2023 2nd International Conference on Electronics, Energy and Measurement (IC2EM 2023)

Low-complexity architecture for Cognitive radio

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***Abstract*—Every day, electromagnetic radio spectrums become precious and expensive. Cognitive radios represent one of the best solutions to improve the available radio frequency (RF) spectrum utilization. Since many forms of communication do not utilize the allocated spectrum fully. So, dynamic detection of no utilized spectrum is crucial. Generally, energy sensing and cyclostationary feature sensing are the most used techniques. Traditional cyclostationary feature-sensing signal correlations are implemented by a complex adder and complex multiplier, which requires significant memory space to store filter coefficients and increased hardware usage. To overcome the above-mentioned problems, a complex pipelined multiply and adder architecture is designed to reduce the area occupancy further. In this research, complex multiplication is designed using two absolute multipliers. The proposed architecture is coded using VHDL on a Virtex-5 Field-Programmable Gate Array (FPGA) device, and the results are compared with similar works. The implementation demonstrates that the proposed operator can reduce FPGA logic requirements with a high maximum working frequency.**

Keywords—5G, Cognitive radio (CR), Finite impulse response Field Programmable Gate Array

I. INTRODUCTION

Software Defined Radio (SDR), which is an implementation of reconfigurable radio, aims to design a universal and versatile communication system capable of supporting different telecommunication standards. In order to achieve this Software Defined Radio goal, this universal system has the ability to be easily reconfigured, configurable or reprogrammable. Software-defined radio, in essence, involves employing a collection of methods that enable the reconfiguration of a communication system without the necessity to alter the hardware components of the system [1]. This advancement allows a single universal circuit to combine functionalities that were previously managed by distinct circuits associated with various radio standards supported by telecommunications equipment [1].

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Cognitive radio (CR) technology represents a progression from software-defined radio (SDR) as it possesses the capability to dynamically reprogram and reconfigure itself.

CR represents an application of intelligent radio, which aims to optimize the use of frequency bands, whether they are licensed or not (when opportunistic radio seeks to use licensed frequencies, it is called opportunistic radio frequency or spatial). In this type of radio, we have an opportunistic network (a secondary network), and an official network (a primary network). A so-called secondary user can at any time access a frequency band of another main user who has a license on this band. The secondary user can only access this band if he finds it free and not occupied by the primary user. Once the service is terminated or the primary user needs to establish a connection, the secondary user will need to release this band. The main operations handled by the CR are the detection and adaptation of the spectrum [2]. To this end, several detection algorithms have been proposed and analyzed [3].

Numerous studies have explored diverse implementations of CR spectrum sensing architectures [6-7-8-9-10]. For instance, the authors in [9] proposed a reconfigurable and architecture of time domain cyclostationary-feature detector (TCD) for spectrum sensing in the cognitive-radio wireless

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network. In their research, a hardware-efficient techniques have been introduced for the multiply-&-accumulate and accumulator architectures of suggested TCD design, aiming to reduce its complexity.

The authors in [10] proposed a MAC that is composed of four real multiplications and two real additions.

Nevertheless, these earlier works exhibit intricate hardware utilization and low-frequency computation.

The subsequent sections of this paper are structured as follows: Section 2 outlines the proposed pipeline architecture for complex multiplication and addition. In Section 3, we assess the performance of the proposed architecture. Finally, Section 4 concludes the paper.

II. Cyclostationary Detection

Cyclostationary feature detection has the potential to identify the core user even when provided with limited information about the signal structure. In order to detect the primary user within the spectral band, it is necessary to identify the periodicity of the received signal.

Commonly, periodicity is established using sinusoidal carriers, pulse trains, spreading codes, pilot sequences, cyclic prefixes, and other repetitive carriers. These periodic signals demonstrate spectral correlation and exhibit periodic statistical properties, as opposed to random noise signals.

Cyclostationary feature detection is particularly effective in low signal-to-noise ratio (SNR) scenarios due to its immunity to noise. However, it does require prior knowledge of the signal to differentiate between the main user signal and the CR transmission signal. Consequently, the cyclostationary signal detection technique is considered favorable as it performs well with minimal information about the signal structure.

A signal x(n) is deemed cyclostationary if its time-varying autocorrelation expectation is periodic and can be expressed as a Fourier series expansion [6].

Figure 1 illustrates a generic block diagram outlining the fundamental operation of the detection scheme. Initially, the input signal x(t) undergoes filtration to mitigate the presence of noise. The resulting signal is then correlated with other captured signals, and the correlation outcome is compared to a predefined threshold, denoted as l. This comparison yields the test statistic result T(x), which ultimately determines the presence or absence of the primary user.

Fig. 1. Block Diagram of CS detection scheme

III. Proposed Pipeline Architecture for Complex Multiplication and Addition

The cyclostationary based sensing technique enhances Primary Users (PUs) detection performance despite its high complexity of implementation and hardware utilization.The cyclostationary employed a correlator to perform both autocorrelation and intercorrelation functions on demand. The core content of the cyclostationary was based on Multiply Accumulation operation (MAC) . In this technique, traditional MAC require a complex multiplier and complex adder takes up a large area in a hardware implementation.

A. Complexe multiplication

A complex multiplier can be realized by four real multiplications and two real additions. Its mathematical form can be expressed as follows:

$$(a + bj)(c + dj) = (ac - bd) + j(bc + ad) \quad (1)$$

This complex multiplier occupies a large area in a hardware implementation (multiplier consumption increases with increasing binary representation of operands). Fortunately, this complex multiplier can be realized with three real multiplications and 5 real additions based on Equation 2:

$$(a + bj)(c + dj) = (ac - bd) + j(bc + ad)$$
$$= \{c(a - b) + b(c - d)\} + j\{d(a + b) + b(c - d)\} \quad (2)$$

It is therefore clear that the architecture with three multiplications, makes it possible to reduce the surface and the electric consumption of the circuit compared to architecture with 4 multiplications, but decreases the maximum frequency of the operation of the butterfly.

To overcome above-mentioned problems, figure two present the proposed pipeline architecture of the Multiply Accumulation operation (MAC) base on pipelined architecture of the complex multiplier and the complex addition.

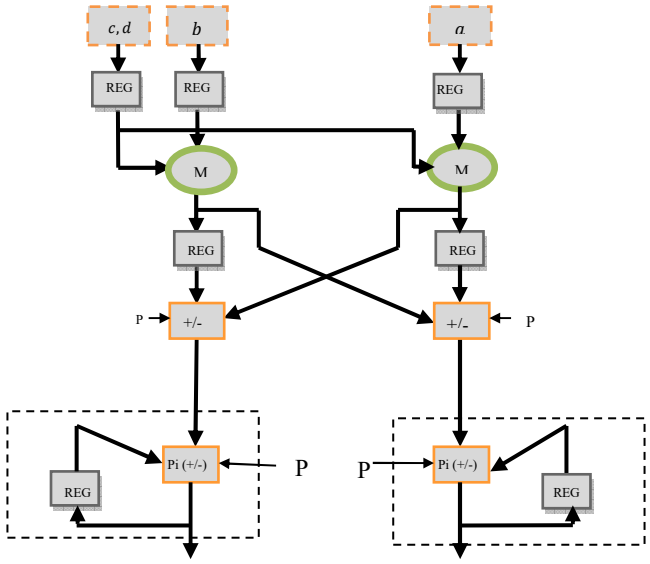

Fig 2. The RTL pipeline architecture for the complex multiplier and accumulator.

This architecture requires only 2 real multipliers; moreover, it allows performing the multiplication operation in 2 clock cycles according to equation 3.

$$\begin{cases} Cycle\ 1: A1 = ac; B1 = bc \\ Cycle\ 2: A2 = ad; B2 = bd \\ real\ part = ac - bd \\ Imaginary\ part = bc + ad \end{cases} \quad (3)$$

B. Accumulator

For the adder in the accumulator, we have proposed a fast pipeline structure adder adapted to this addition operation. Their internal architecture is composed of three adders and registers. One adder for calculating the high point sum (MSB) for the two inputs, one adder for calculating the low point sum (LSB) for the two inputs, and the third adder calculates the sum of the result of the first adder(MSB) and restraint (Figure 3).

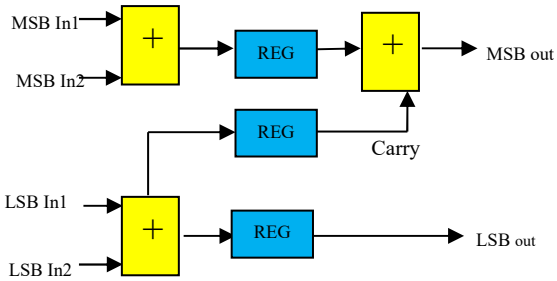

Fig. 3: The pipeline architecture of the adder.

IV. FPGA IMPLEMENTATION, RESULTS AND PERFORMANCE COMPARISONS

The proposed architecture's RTL description has been successfully implemented on Xilinx Virtex- V FPGA [11] using VHDL (VHSIC Hardware Description Language) structural description. The digital implementation was performed using Xilinx ISE 10.1i [12] tool to determine logic resource requirements and real-time constraints.

The evaluation of the architecture's performance and FPGA resources was compared with similar existing works from the literature. The synthesis results, presented in Table 1, showcase the maximum frequency and hardware resources consumption in terms of slices. The results demonstrate that the proposed universal architecture can be efficiently implemented in real-time on FPGA technology, reducing overall complexity. It strikingly achieves an attractive tradeoff between high speed and low logic resources. For instance, the logic implementation requires only 22CLB-Slices with no multipliers or DSP blocks, and no RAM blocks under the maximum operating frequency of 457.907 MHz. To provide a comprehensive evaluation, the implementation results were compared with previous works that share the same target functionality [9,10], utilizing FPGA Virtex 5 and VHDL for direct comparison of all results.

Table 1. Implementation results on XC5VLX20T Virtex-V FPGA of the proposed architecture and previous works.

Device	Architecture	Slices	Flipflops	LUT	Number of DSP48Es	Frequency (MHz)	Power (W)
Virtex 5	MAC (four M) [9]	8	8	8	4	126.215	0.321
Virtex 5	MAC [10]	48	48	49	2	583.311	0.322
Virtex 5	Proposed MAC	32	16	32	2	174.268	0.321

Figs. 4 and 5 present the RTL synthesis results of the performed FPGA implementations ofour architecture.

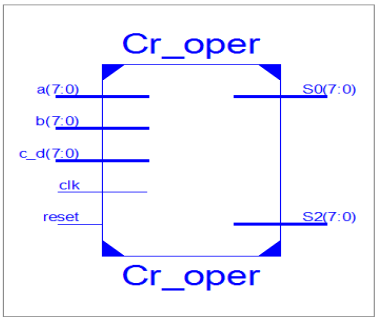

Fig. 4: Top level of the proposed module.

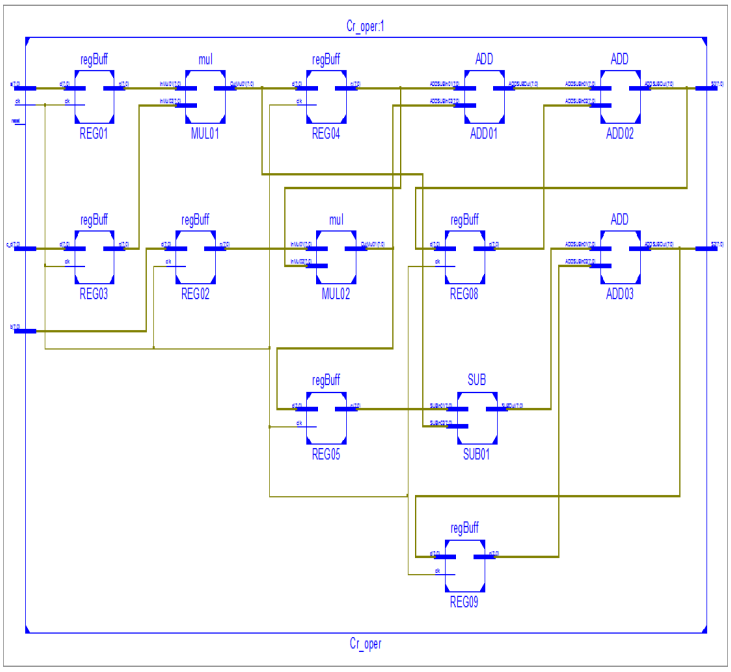

Fig. 5 RTL diagrams of the implementation on FPGA Virtex V of the proposed architecture.

Thus, as it is shown in the table 1, our architecture operates at minimum more 174MHz.

From the comparisons, the proposed architectures are efficient in terms DSP48E requirements if compared against[9] and [10] architectures, it saves two DSP48E compared to [9]. However, requires more LUTs than in [9].

Thus, the implementation results clearly demonstrate that our proposed architecture can deliver a reduction of the total FPGA logic area requirement, and the execution time of the FPGA implementation. The power consumed by the architecture was estimated by XPower analyzer, Xilinx tool, after the place and route process. Comparison of our proposed with the architecture proposed in [10] in terms of power consumption, reveals that our proposed architecture achieve appropriate power.

V. CONCLUSION

The challenges related to spectrum sensing are steadily rising due to the growing adoption of CR technology. CR plays a crucial role in enhancing spectrum efficiency and effectiveness. In this study, pipeline architecture was introduced for complex multiplication and addition-based spectrum sensing in CR. The pipeline employs complex multiplication and adder components to design the correlation. To ascertain the effectiveness of our approach, we implemented the proposed architecture using VHDL structural description on Xilinx Virtex V-FPGA technology. The results unequivocally prove that our architecture substantially reduces the FPGA logic are requirements. Additionally, compared to previous works, implementing our architecture consumes fewer FPGA hardware resources, reinforcing its efficiency and superiority.

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